## REMARKS

In the Official Action mailed **June 8, 2001**, the Examiner reviewed claims 1-20. Claims 1, 2, 7, 8, 10, and 20 were rejected under 35 U.S.C. §102(b), as being anticipated by Dea (USPN 5,469,208, hereinafter "Dea"). Claims 3, 4, 5, and 12 were rejected under 35 U.S.C. 103 (a) as being unpatentable over Dea. Claims 6 and 13-17 were rejected under 35 U.S.C. 103 (a) as being unpatentable over Dea in view of Abramatic et al. (USPN 4,546,383, hereinafter "Abramatic"). Claim 9 was rejected under 35 U.S.C. 103(a) as being unpatentable over Dea in view of Yan (USPN 5,438,374, hereinafter "Yan"). Claim 11 was rejected under 35 U.S.C. 103(a) as being unpatentable over Dea in view of Hardiman (USPN 5,923,223, hereinafter "Hardiman"). Claim 18 was rejected under 35 U.S.C. 103(a) as being unpatentable over the system of Dea and Abramatic as applied to claim 13 above, and further in view of Yan. Claim 19 was rejected under 35 U.S.C. 103(a) as being unpatentable over the system of Dea and Abramatic as applied to claim 13 above, and further in view of Hardiman.

### Rejections under 35 U.S.C. §102(e) and §103(a)

Independent claim 1 and 20 were rejected as being anticipated by Dea and independent claim 13 was rejected as being unpatentable over Dea in view of Abramatic. Applicant respectfully points out that Dea is directed to a compression/decompression accelerator **coupled to a system bus** (See Dea, Fig. 1). In contrast, the present invention discloses a graphics controller **within a core logic unit** (See Fig. 2, and page 8, lines 4-6 of the instant application). A core logic unit is circuitry within a computer system that interfaces a processor to a memory and a peripheral bus and performs other functions (See page 5, lines 12-13 of the instant application). Specifically, the core logic unit in the present

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invention includes the graphics controller and the circuitry of north bridge 118 (see page 8, line 5 of the instant application).

Including the graphics controller into the core logic unit is advantageous because communications between the graphic controller and the core logic elements remain within the core logic unit and are therefore faster than when these communications pass through a system bus. Performing these communications across the system bus is slower because system bus bandwidth is typically less than the bandwidth within the core logic unit, and because of system bus contention with other peripheral devices. There is no suggestion, either explicit or implicit, within Dea, or within Dea in combination with Abramatic, to include the graphics controller within the core logic unit.

Accordingly, Applicant has included the limitations of dependent claims 8 and 17 into independent claims 1 and 13, respectively to clarify that the graphics controller is included within the core logic unit. Independent claim 20 has also been amended to clarify that the graphics controller is included within the core logic unit. Dependent claims 8 and 17 have been cancelled without prejudice.

Hence, Applicant respectfully submits that independent claims 1, 13, and 20 as presently amended are in condition for allowance, and that claims 2-7 and 9-12, which depend upon claim 1, and claims 14-16 and 18-19, which depend on claim 13, are for the same reasons in condition for allowance and for reasons of the unique combinations recited in such claims.

**The claims:**

1       1. (Once Amended) An apparatus for compressing video data, comprising:

2       a video input port, for receiving video data for a current video frame;

3       a video input buffer coupled to the video input port, for storing video data

4 from the video input port;

5       a previous frame buffer, for storing at least a portion of a previous video

6 frame;

7       an operation unit coupled to the video input buffer and the previous frame

8 buffer, for performing an operation between data from the video input buffer and

9 data from the previous frame buffer; and

10       a result buffer coupled to the operation unit, for storing the result of an

11 operation from the operation unit;

12       <u>wherein the apparatus resides inside of a core logic chip for a computer</u>

13 <u>system</u>.


1       13. (Once Amended) An apparatus for compressing video data,

2 comprising:

3       a video input port, for receiving video data for a current video frame;

4       a video input buffer coupled to the video input port, for storing video data

5 from the video input port;

6       a previous frame buffer, for storing at least a portion of a previous video

7 frame;

8       an exclusive-OR unit coupled to the video input buffer and the previous

9 frame buffer, for performing an exclusive-OR operation between data from the

10 video input buffer and data from the previous frame buffer;

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11        a result buffer coupled to the operation unit, for storing the result of an

12        operation from the operation unit;

13        a memory port coupled to the previous frame buffer and the result buffer,

14        for transferring data to and from a memory that stores video data from the video

15        input port and result data from the result buffer; and

16        a memory coupled to the memory port for storing the video data from the video

17        input port and result data from the result buffer, wherein the video data is stored to

18        in a current frame in the memory and the result data is stored in a difference frame

19        in the memory;

20        <u>wherein the apparatus resides inside of a core logic chip for a computer</u>

21        <u>system</u>.


1        20. (Once Amended) A computer system including resources for

2        compressing video, comprising:

3        a central processing unit within the computer system;

4        a video input port, for receiving video data for a current video frame;

5        a video input buffer coupled to the video input port, for storing video data

6        from the video input port;

7        a previous frame buffer, for storing at least a portion of a previous video

8        frame;

9        an operation unit coupled to the video input buffer and the previous frame

10        buffer, for performing an operation between data from the video input buffer and

11        data from the previous frame buffer; and

12        a result buffer coupled to the operation unit, for storing the result of an

13        operation from the operation unit;

14        <u>wherein the video input port, the video input buffer, the previous frame</u>

15        <u>buffer, the operation unit, and the result buffer reside inside of a core logic chip</u>

16        <u>for the computer system</u>.

## CONCLUSION

It is submitted that the present application is presently in form for allowance. Such action is respectfully requested.

Respectfully submitted,

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